	Applicati n N .	Applicant(s)
Notice of Allowability	10/710,597	LAI, HAN-CHUNG
	Examiner	Art Unit
	Ida M. Soward	2822
The MAILING DATE of this communication appeall claims being allowable, PROSECUTION ON THE MERITS IS nerewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIPORT OF THE OFFICE OF UPON PETITION BY THE APPLICANT. See 37 CFR 1.313	(OR REMAINS) CLOSED in this apport or other appropriate communication GHTS. This application is subject to and MPEP 1308.	plication. If not included will be mailed in due course. <b>THIS</b>
1. X This communication is responsive to <i>the Applicant's amendment filed March 16, 2006</i> .		
2. X The allowed claim(s) is/are <u>1-16</u> .		
3.  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a)  All b)		
Attachm nt(s)  I. Notice of References Cited (PTO-892)  I. Notice of Draftperson's Patent Drawing Review (PTO-948)  Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date  I. Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. Interview Summary Paper No./Mail Dat 8), 7. Examiner's Amenda 8. Examiner's Stateme 9. Other	ie
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## **DETAILED ACTION**

This Office Action is in response to the Applicant's amendment filed March 16, 2006.

## Allowable Subject Matter

Claims 1-16 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims, such as:

In claim 1, "a plurality of scan lines disposed over the substrate; a plurality of data lines disposed over the substrate. wherein the substrate is defined into a plurality of pixel area by the scan lines and the data lines; a plurality of thin film transistors driven by the scan line: and the data lines, wherein each thin film transistor is disposed in one of the pixel areas correspondingly; an etching stop layer disposed over the scan lines, wherein the etching stop layer has a plurality of openings; and a plurality of pixel electrodes, each pixel electrode is disposed in one of the pixel areas and is electrically connected to one of the thin film transistors correspondingly, wherein a portion of each pixel electrode is coupled to one of the scan lines through one of the openings to form a storage capacitor"; and

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In claim 9, "a plurality of scan lines disposed over the substrate; a plurality of data lines disposed over the substrate, wherein the substrate is defined into a plurality of pixel areas by the scan lines and the data lines; a plurality of thin film transistors driven by the scan lines and the data lines, wherein each thin film transistor is disposed in one of the pixel areas correspondingly; a plurality of common lines disposed over the substrate, wherein each common line is located between two adjacent scan lines; an etching stop layer disposed over the common lines. wherein the etching stop layer has a plurality of openings: and a plurality of pixel electrodes each pixel electrode is disposed in one of the pixel areas and is electrically connected to one of the thin film transistors correspondingly, wherein a portion of each pixel electrode is coupled to one of the scan lines through one of the openings to form a enrage capacitor".

The dependent claims being further limiting and definite are also allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

## **Conclusion**

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to thin film transistor arrays:

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Ahn et al. (US 2001/0031510 A1)

Chen et al. (US 6,362,028 B1)

Dai et al. (US 6,989,299 B2)

Huang (US 6,714,269 B1)

Liao et al. (US 2004/0140469 A1)

Matsueda (5,173,792)

Possin et al. (5,041,888)

Tsai et al. (5,959,312)

Wu (5,828,082).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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IMS

May 30, 2006

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